Revision History

Revision	*Date*	*Modifier*	*Description*
0.93	2010/7/8	Cliff	Initial version
0.94	2010/7/13	James	IO pin definition refine
0.95	2010/7/24	Cliff	Add timing chart
0.96	2010/7/28	Samuel	Add marking rule
0.97	2010/8/3	Samuel	Revise pin definitions
0.98	2010/8/20	Samuel	Modify pins
0.99	2010/8/24	Samuel	Modify pins
0.992	2010/9/7	Samuel	Add CCIR656 & CCIR601 definitions
0.994	2010/9/23	Jessica, James, Paul	Update the functional description.
0.995	2010/9/29	Cliff, Samuel	Add layout guide. Modify pins
0.996	2010/9/29	Paul	Update DC specifications
0.997	2010/10/26	Samuel	Modify pins
0.998	2010/11/1	Samuel	Exchange Chip_type and Boot_type pins
0.999	2010/11/5	Samuel	Add power on sequence
1.000	2010/11/9	Samuel	Modify pins
1.001	2010/11/19	Samuel	Modify marking rule
1.002	2010/12/2	Samuel	Modify GPIO pins
1.003	2011/1/19	Samuel	Add SPI
1.004	2011/1/26	Samuel	Modify pin A16
1.005	2011/3/14	Samuel	Add NA pins
1.006	2011/3/16	Samuel	Revise SD20 & SD22 pins
1.007	2011/3/30	Samuel	Exchange pins # H3 & G3
1.008	2011/3/31	Samuel	Add Reflow Condition
1.009	2011/4/27	Samuel	Modify PVDDIO_USB & PVSSIO_USB pins
1.010	2011/5/30	Samuel	Add RGB666
1.011	2011/7/29	Jesse	-remove CCIR656, CCIR601 -remove USB
1.012	2012/4/24	Samuel	Modify pins
1.013	2012/11/9	Pearl	Modify P.26 Pad Power Supply, the Max value from 3.36 to 3.63
1.014	2013/4/17	James	Add SMT Assembly Recommendations

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1. Description

TF-680 is a single chip video streaming SoC that includes video codec and up to 7.1 channels audio. TF-680 supports network connectivity via SDIO or Ethernet interface that enables the different connection methods. TF-680 compresses video and audio data and transmits them to Ethernet or WiFi. It can also decompress video and audio data from WiFi or Ethernet and display them on a TV. Image engine in TF-680 compresses video into MJPEG format and the support resolution of video can be up to 1920x1080 resolution. It decompresses MJPEG files and delivers video to a display. Comparing with other compression methods such as MPEG1/2/4 and H.264, MJPEG delivers very low latency bidirectional interactive mechanism which is the best solution for interactive applications. Lip sync mechanism also designed in the TF-680 guarantees video and audio are in sync.

TF-680 embeds scalar engine that can scale down the captured pictures and then transmits them into network under limited network bandwidth.

Two UART, one I2C and one DDC are used for control purpose. Either controller or I2S controller are dedicated for audio input and I2S interface supports up to 7.1 channels audio. The ICE interface provides the easiest way for software engineer to develop firmware and debug it. Ethernet MAC is included in TF-680.

TF-680 has one IR which can be receivers or transmitters. TF-680 has two embedded PLL, one is to generate different timing for different resolution display requirements and the other one is dedicated for SDRAM high performance operations.

2. Features

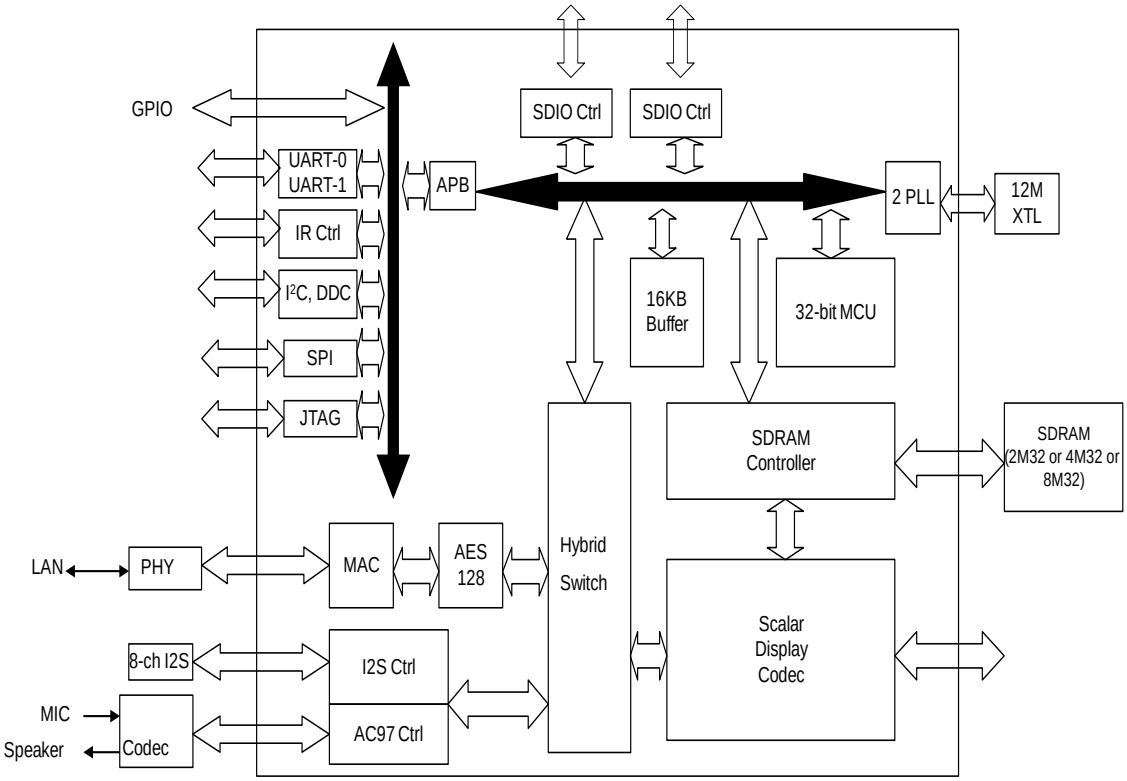
- **MCU**
  - 32-bit MCU, 160MHz operating frequency
  - 8KB instruction cache and 8KB memory cache
  - 19 multi-functions GPIO ports
- **Image compression / decompression engine, 166MHz operating frequency**
  - Encode/decode image from 16 x 16 to 2M pixel image
  - Input image format
    RGB 888
  - Output image format
    RGB 888
    RGB 666
  - Image size: supports up to 2M pixel image resolution including the following popular resolutions
    640X480 @ 85fps
    800X600 @ 85fps
    1024X768 @ 75fps
    1280X1024 @ 60fps
    1600X1200 @ 30fps
    720X480 @ 60fps
    1280X720 @ 60fps
    1920X1080 @ 30fps
- **Scalar**
  - Scale up to any size, maximum resolution up to 2048x2048
  - Scale down to any size
- **Supports**

- RMII, MII or Turbo MII interface
- 802.3x jamming control for full duplex mode and Jamming for half duplex mode

3. System block diagram

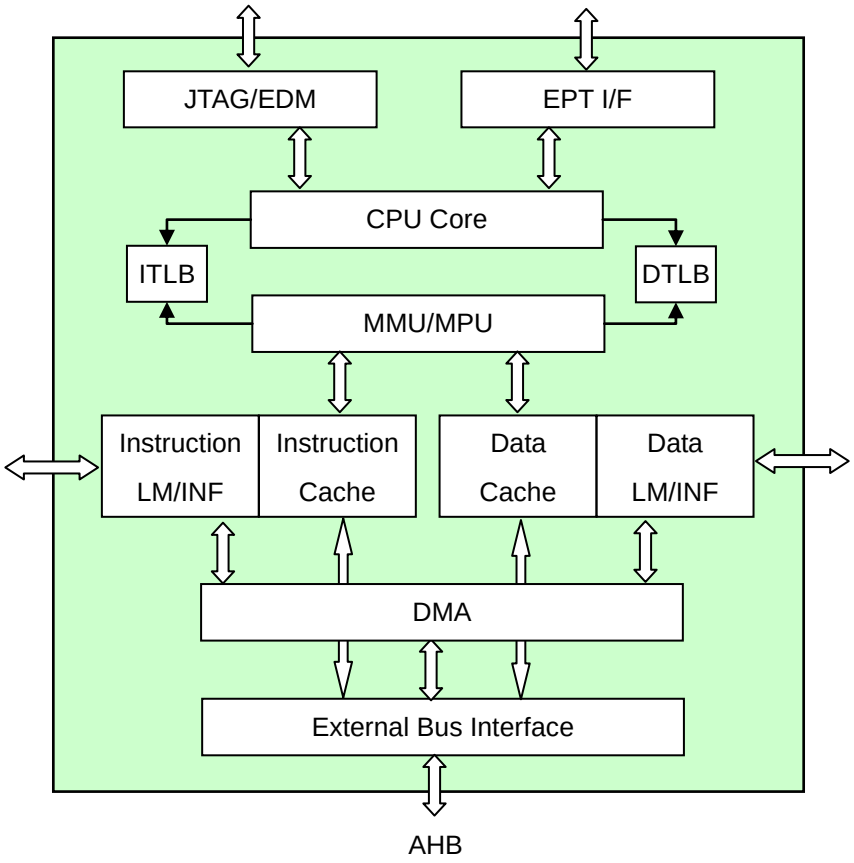
4. Functional Descriptions

Below figure shows the internal block diagram of TF-680.



4.1 MCU

The MCU is 32-bit, 5-stage pipeline CPU core with 160MHz operating frequency. The MCU has two caches, one is instruction cache and the other is data cache. Both are 8Kbytes. MMU (Memory Management Unit) is also supported for address conversion. The block diagram is as below. The detail information of MCU refers to the programming guide.



4.2 Video Interface

TF-680 video interface provides RGB888 for video input while TF-680 is configured as video encoder mode, and RGB888 and RGB666 for video output while TF-680 is configured as video decoder mode. For encoder mode, video data and control signals are sampled referring video clock VCLK. In decoder mode, video data and control signals are driven referring video clock VCLK. The maximum frequency of VCLK is 165MHz.

4.3 Scalar

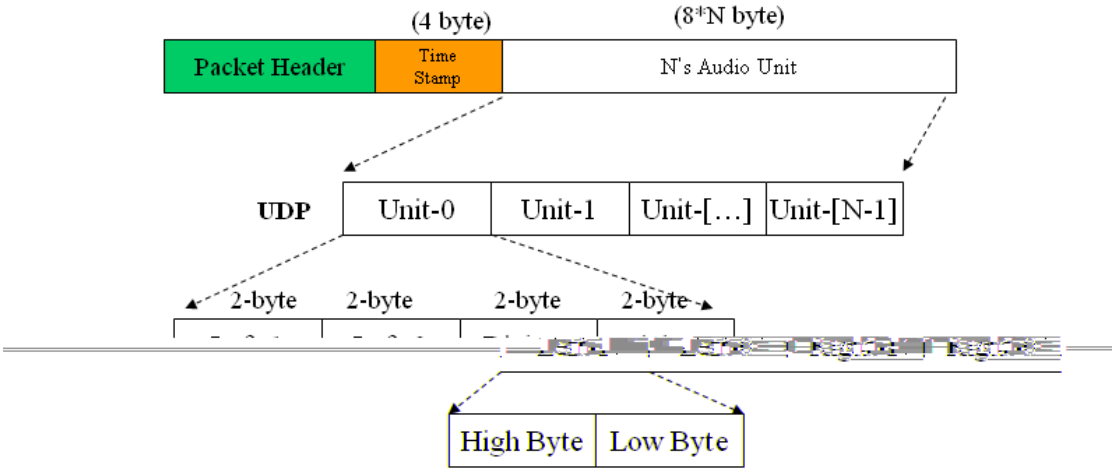
TF-680 Scalar provides scaling down and up capability for video resolution adjustment to satisfy display and network bandwidth requirements. In encoder mode, the Scalar only provides scaling down capability to reduce data bandwidth to satisfy the low network bandwidth requirements. In decoder mode, the Scalar provides scaling down and up capability to satisfy display requirements.

4.4 SDRAM

TF-680 SDRAM interface supports the max access SDRAM size up to 32Mx32. To support 1080P video resolution compression/decompression, the minimum size of SDRAM is 4Mx32. If maximum video resolution is only up 720P, 2Mx32 SDRAM will be sufficient. The SDRAM interface is operating at 160MHz.

4.5 AC 97 Interface

TF-680 AC 97 interface provides Standard AC-Link interface. Bit clock frequency is 12.288MHz. The AC 97 interface provides a bridge between external audio codec and the internal AC 97 controller. AC 97 interface supports audio format 2-channel, 16-bit only. The audio data format inside TF-680 is as bellow. The Packet Header is configurable and it can be Ethernet MAC header data or UDP data. The Time Stamp is used for synchronization between sender and receiver and it must be zero if it is not adopted.



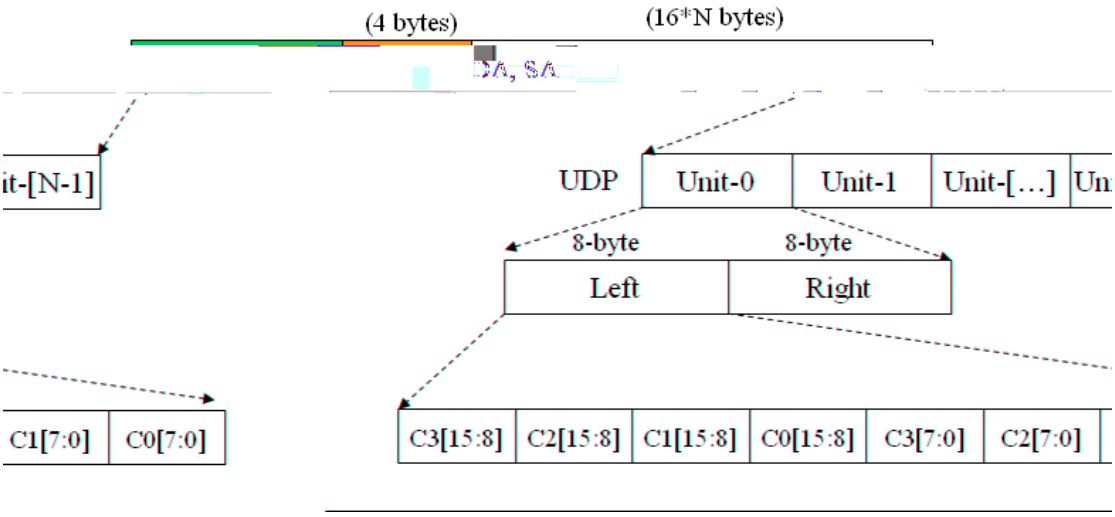
4.6 I2S Interface

TF-680 I2S interface supports 4 audio data format as bellows.

- 2 channels, 16 bits, 48K
  I2S clock frequency is 2 * 16 * 48000 = 1536000 Hz
- 2 channels, 24 bits, 48K
  I2S clock frequency is 2 * 32 * 48000 = 3072000 Hz
- 8 channels, 16 bits, 48K
  I2S clock frequency is 2 * 16 * 48000 = 1536000 Hz
- 8 channels, 24 bits, 48K

I2S clock frequency is 2 * 32 * 48000 = 3072000 Hz

The data format inside TF-680 for 8-channel, 16-bit is shown as bellow. The same as AC 97 interface, the Packet Header is configurable and it can be Ethernet MAC header data or UDP data. The Time Stamp is used for synchronization between sender and receiver and it must be zero if it is not adopted.



4.7 SPI Interface

TF-680 SPI interface provides firmware execute in or download from external serial SPI flash. When TF-680 is configured to this mode through power on strap pin, TF-680 executes firmware in external serial SPI flash or downloads firmware from external serial SPI flash to memory. The SPI initial clock frequency is 1MHz. It can be adjust to 13.3MHz by setting the internal register. TF-680 does not supply SPI device mode.

4.8 SDIO Interfaces

TF-680 SDIO interfaces support two SDIO interfaces, one supports host mode, and the other supports slave mode. In the SDIO host mode interface, TF-680 provides 48MHz clock output. For SDIO device mode interface, it accepts max up to 50MHz clock input. Both are support 1-bit and 4-bit data modes.

4.9 High Speed UART (Bluetooth UART)

TF-680 High Speed UART interface provides a partial set of modem control pins, including nCTS and nRTS. It can support baud rates up to 1152Kbps. The High Speed UART features include:

- High-speed NS 16C550A-compatible UART
- Programmable baud rates up to 1152Kbps.
- Ability to add or delete standard asynchronous communication bits (start, stop, and parity0 in serial data.
- Programmable baud rate generator that allows the internal clock to be divided by 1 to (216-1) to generate an internal16X clock
- Fully programmable serial interface:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, and no parity detection
  - 1-, 1.5-, or 2-stop bit generation
- Complete status reporting capability
- Ability to generate and detect line breaks
- Fully prioritized interrupt system controls
- Separate DMA requests for data transmission and reception services
- Break, parity, overrun, framing error simulation for UART mode
- BTUART provides 32-byte transmit FIFO and 32-byte receive FIFO
- STUART provides 16-byte transmit FIFO and 16-byte receive FIFO

4.10 Standard UART

It is the same as High speed UART. But it does not include the modem control pins.

4.11 IR Receiver

TF-680 IR Receiver provides a input pin to receive external IR signal to remote control remote devices. It supports 38KHz and 56KHz IR signal with external IR detector module.

4.12 I2C Interface

TF-680 I2C interface provides two operation modes, one is I2C master and the other is slave mode. For slave mode, it allow external device directly access the internal chip resources with internal MCU to intervene. It can support up to 400kbps.

4.13 DDC

The operation is the same as I2C.

4.14 10/100Mbps Ethernet MAC

TF-680 builds in a 10/100Mbps Ethernet MAC with MII, RMII and Turbo MII interfaces for connection with a physical layer device (PHY). TF-680 10/100Mbps Ethernet MAC interface also provides serial management interface to read/write registers of PHY. The MAC supports IEEE802.3x flow control for full duplex mode and jamming flow control mechanism for half duplex mode. When 10/100Mpbs Ethernet MAC interface is configured in RMII or Turbo MII mode, the clock frequency is 50MHz and it is driven by external device.

4.15 GPIO

TF-680 provides a lot of programmable input/output pins (GPIO) for system level applications and usages. Each GPIO can be programmed as an input or output. This GPIO can also be an interrupt input, and it supports at the rising edge, falling edge, and high/low level interrupt sense types. The each port of GPIO can be independently programmed. All these GPIOs are controlled by the module GPIO Controller. The GPIO Controller is clocked by an 80MHz APB clock.

4.16 PLL

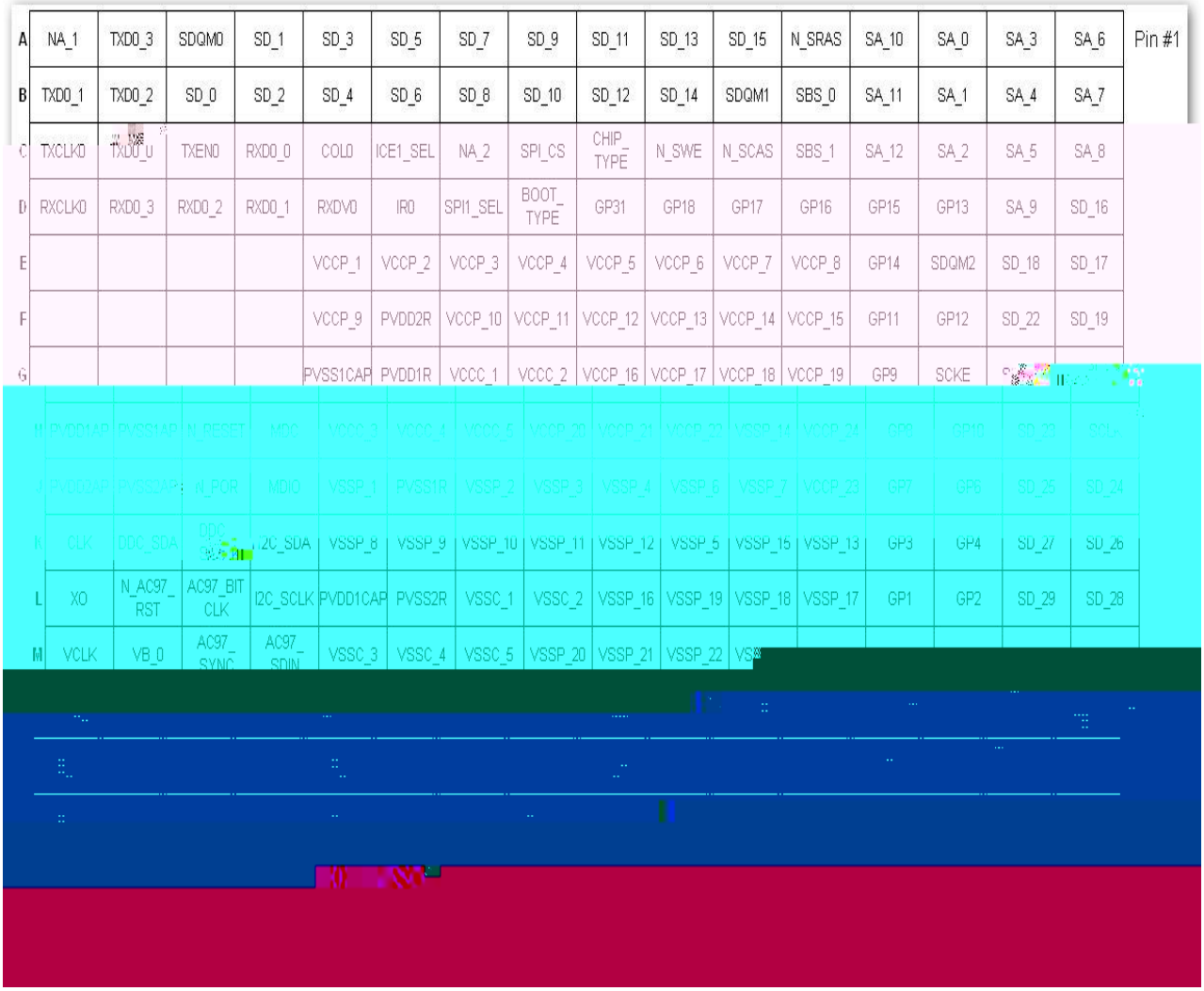
TF-680 clock is sourced by external 12MHz crystal and internal PLL generates different frequencies for internal different modules usage. PLL generates xxxx, xxxMHz, and xxxMHz frequencies. The maximum of the frequency generated by PLL is 480MHz. The external crystal specifications include:

- Period Jitter: RMS = 25 ps, PK-PK = 250 ps. Duty cycle: 45 ~ 55 %.
- Locking time = 0.5 ms.

4.17 PWM Interface

TF-680 supports two PWM signals that provide output frequency from 1.25kHz to 80MHz for LED backlight control. It also provides register to configure the duty-cycle of PWM.

5. Pin Descriptions



A	NA_1	TXD0_3	SDQM0	SD_1	SD_3	SD_5	SD_7	SD_9	SD_11	SD_13	SD_15	N_SRAS	SA_10	SA_0	SA_3	SA_6	Pin #1
B	TXD0_1	TXD0_2	SD_0	SD_2	SD_4	SD_6	SD_8	SD_10	SD_12	SD_14	SDQM1	SBS_0	SA_11	SA_1	SA_4	SA_7	
C	TXCLK0	TXD0_0	TXEN0	RXD0_0	COL0	ICE1_SEL	NA_2	SPI_CS	CHIP_TYPE	N_SWE	N_SCAS	SBS_1	SA_12	SA_2	SA_5	SA_8	
D	RXCLK0	RXD0_3	RXD0_2	RXD0_1	RXDV0	IR0	SPI1_SEL	BOOT_TYPE	GP31	GP18	GP17	GP16	GP15	GP13	SA_9	SD_16	
E					VCCP_1	VCCP_2	VCCP_3	VCCP_4	VCCP_5	VCCP_6	VCCP_7	VCCP_8	GP14	SDQM2	SD_18	SD_17	
F					VCCP_9	PVDD2R	VCCP_10	VCCP_11	VCCP_12	VCCP_13	VCCP_14	VCCP_15	GP11	GP12	SD_22	SD_19	
G					PVSS1CAP	PVDD1R	VCCC_1	VCCC_2	VCCP_16	VCCP_17	VCCP_18	VCCP_19	GP9	SCKE			
H	PVDD1AP	PVSS1AP	N_RESET	MDC	VCCC_3	VCCC_4	VCCC_5	VCCP_20	VCCP_21	VCCP_22	VSSP_14	VCCP_24	GP8	GP10	SD_23	SCLK	
J	PVDD3AP	PVSS3AP	N_POR	MDIO	VSSP_1	PVSS1R	VSSP_2	VSSP_3	VSSP_4	VSSP_6	VSSP_7	VCCP_23	GP7	GP6	SD_25	SD_24	
K	CLK	DDC_SDA	DDC_SCL	I2C_SDA	VSSP_8	VSSP_9	VSSP_10	VSSP_11	VSSP_12	VSSP_5	VSSP_15	VSSP_13	GP3	GP4	SD_27	SD_26	
L	XO	N_AC97_RST	AC97_BITCLK	I2C_SCLK	PVDD1CAP	PVSS2R	VSSC_1	VSSC_2	VSSP_16	VSSP_19	VSSP_18	VSSP_17	GP1	GP2	SD_29	SD_28	
M	VCLK	VB_0	AC97_SYNC	AC97_SDIN	VSSC_3	VSSC_4	VSSC_5	VSSP_20	VSSP_21	VSSP_22	VSS						

I/O Type Convention

Except signals **SCLK** and **VCLK** with 12mA driving output, all output signals are 8mA driving strength.

Type	Description
I/O	Bi-directional input and output
I	Input
O	Output
OD	Open Drain
IPU	Internal Pull-Up
IPUC	Controllable internal Pull-Up

Pin	No	Type	Description
N_RESET	H14	I	chip reset
N_POR	J14	I	power on reset
CLK	K16	I	12MHz for PLL
XO	L16	O	clock output pad for crystal
PVDD1AP	H16	I	PLL analog 3.3V power supply
PVSS1AP	H15	I	PLL analog ground supply
PVDD2AP	J16	I	PLL analog 3.3V power supply
PVSS2AP	J15	I	PLL analog ground supply
PVDD1CAP	L12	I	PLL digital 1.2V power supply
PVSS1CAP	g12	I	PLL digital ground supply
PVDD1R	G11	I	1.2V power supply
PVSS1R	J11	I	Ground supply
PVDD2R	F11	I	3.3V power supply
PVSS2R	L11	I	Ground supply
VCCC_n	G9, G10, H10, H11, H12		1.2V power supply (n=1~5)
VCCP_n	E5, E6, E7, E8, E9, E10, E11, E12, F5, F6, F7, F8, F9, F10, F12, G5, G6, G7, G8, H5, H7, H8, H9, J5		3.3V power supply (n=1~24)
VSSP_n	H6, J6, J7, J8, J9, J10, J12, K5, K6, K7, K8, K9, K10, K11, K12, L5, L6, L7, L8, M5, M6, M7, M8, M9		Ground supply (n=1~24)
VSSC_n	L9, L10, M10, M11, M12		Ground supply (n=1~5)
NA_n	A16, C10		Not available (n=1~2) A16 must be connected to ground via a 4.7Kohm resistor.
NC	A16, C10, E13, E14, E15, E16, F13, F14, F15, F16, G13, G14, G15, G16		

CPU I/F

Pin	No	Type	Description
GP0/ SPI_CLK	N6	IPUC/O	bit 0 of GPIO port group 1 SPI clock output
GP1/ SPI_DI	L4	IPUC/O	bit 1 of GPIO port group 1 SPI data input

GP2/ EDM_TMS	L3	IPUC/O	bit 2 of GPIO port group 1 EDM TMS input
GP3/ EDM_TCK	K4	IPUC/O	bit 3 of GPIO port group 1 EDM TCK input
GP4/ EDM_TDI	K3	IPUC/O	bit 4 of GPIO port group 1 EDM TDI input
GP5/ EDM_TRST	M4	IPUC/O	bit 5 of GPIO port group 1 EDM TRST input
GP6/ EDM_TDO	J3	IPUC/O	bit 6 of GPIO port group 1 EDM TDO output
GP7/ EDM_GOICE	J4	IPUC/O	bit 7 of GPIO port group 1 EDM GOICE input
GP8/ EDM_DBGACK	H4	IPUC/O	bit 8 of GPIO port group 1 EDM DBGACK output
GP9/ SD0_WP	G4	IPUC/O	bit 9 of GPIO port group 1 SD0 alternative write protect
GP10/ SD0_CD	H3	IPUC/O	bit 10 of GPIO port 1 SD0 alternative card detect
GP11	F4	IPUC/O	bit 11 of GPIO port group 1
GP12	F3	IPUC/O	bit 12 of GPIO port group 1
GP13/ I2S1_WS	D3	IPUC/O	bit 13 of GPIO port group 1 I2S1 word select output
GP14/ I2S1_SCK	E4	IPUC/O	bit 14 of GPIO port group 1 I2S1 sample clock output
GP15/ I2S1_SD0	D4	IPUC/O	bit 15 of GPIO port group 1 I2S1 sample data lane-0 output
GP16/ PS2SDA1/ I2S1_SD1	D5	IPU/O	bit 16 of GPIO port group 1 PS2_1 data I2S1 sample data lane-1 output
GP17/ PS2CLK1/ I2S1_SD2	D6	IPUC/O	bit 17 of GPIO port group 1 PS2_1 clock I2S1 sample data lane-2 output
GP18/ I2S1_SD3	D7	IPUC/O	bit 18 of GPIO port group 1 I2S1 sample data lane-3 output

MII/RMII/Turbo-MII

Pin	No	Type	Description
TXCLK0	C16	I/O	Transmission clock MII/RMII/Turbo-MII tx_clk input
TXD0_0	C15	O	bit 0 of transmission data bus MII/RMII/Turbo-MII txd0 output
TXD0_1	B16	O	bit 1 of transmission data bus MII/RMII/Turbo-MII txd1 output
TXD0_2	B15	O	bit 2 of transmission data bus MII/Turbo-MII txd2 output
TXD0_3	A15	O	bit 3 of transmission data bus MII/Turbo-MII txd3 output
RXCLK0	D16	I	Received clock MII/RMII/Turbo-MII rx_clk input
RXD0_0	C13	I	bit 0 of received data bus MII/RMII/Turbo-MII rxd0 input
RXD0_1	D13	I	bit 1 of received data bus MII/RMII/Turbo-MII rxd1 input
RXD0_2	D14	I	bit 2 of received data bus MII/Turbo-MII rxd2 input
RXD0_3	D15	I	bit 3 of received data bus MII/Turbo-MII rxd3 input
RXDV0	D12	I	Receive data valid MII/RMII/Turbo-MII rx_dv input
COL0	C12	I	MII/RMII/Turbo-MII Collision indication
TXEN0	C14	O	Transmission enable
MDC	H13	O	Management data clock
MDIO	J13	I/O	Management data input/output

Video I/F

Pin	No.	Type	Description
VCLK	M16	I/O	pixel clock for RGB pixel clock for YCbCr
VVSYNC	P10	I/O	vertical sync
VHSYNC	N10	I/O	horizontal sync
VRGB_VALID	T9	I/O	pixel data valid
SRC_HS	P8	I	source Hsync

SRC_VS	R9	I	source Vsync
VR_0	P12	I/O	bit 0 (the lowest bit) of pixel red color
VR_1	R12	I/O	bit 1 of pixel red color (RGB888)
VR_2	T12	I/O	bit 2 of pixel red color (RGB888) bit 0 (the lowest bit) of pixel red color (RX : RGB666)
VR_3	P11	I/O	bit 3 of pixel red color (RGB888) bit1 of pixel red color (RX : RGB666)
VR_4	R11	I/O	bit 4 of pixel red color (RGB888) bit 2 of pixel red color (RX : RGB666) bit 8 of 12-bit transfer pixel color (RX)
VR_5	T11	I/O	bit 5 of pixel red color (RGB888) bit 3 of pixel red color (RX : RGB666) bit 9 of 12-bit transfer pixel color (RX)
VR_6	T10	I/O	bit 6 of pixel red color (RGB888) bit 4 of pixel red color (RX : RGB666) bit 10 of 12-bit transfer pixel color (RX)
VR_7	R10	I/O	bit 7 (the highest bit) of pixel red color (RGB888) bit 5 (the highest bit) of pixel red color (RX : RGB666) bit 11 of 12-bit transfer pixel color (RX)
VG_0	R15	I/O	bit 0 (the lowest bit) of pixel green color (RGB888)
VG_1	R14	I/O	bit 1 of pixel green color (RGB888)
VG_2	T16	I/O	bit 2 of pixel green color (RGB888) bit 0 (the lowest bit) of pixel green color (RX : RGB666)
VG_3	T15	I/O	bit 3 of pixel green color (RGB888) bit 1 of pixel green color (RX :

			RGB666)
VG_4	T14	I/O	bit 4 of pixel green color (RGB888) bit 2 of pixel green color (RX : RGB666)
VG_5	P13	I/O	bit 5 of pixel green color (RGB888) bit 3 of pixel green color (RX : RGB666) bit 5 of 12-bit transfer pixel color (RX)
VG_6	R13	I/O	bit 6 of pixel green color (RGB888) bit 4 of pixel green color (RX : RGB666) bit 6 of 12-bit transfer pixel color (RX)
VG_7	T13	I/O	bit 7 (the high) re.85 1_ b(x)4(t)TJETC

			(RX)
VB_6	P14	I/O	bit 6 of pixel blue color (RGB888) bit 4 of pixel blue color (RX : RGB666) bit 2 of 12-bit transfer pixel color (RX)
VB_7	R16	I/O	bit 7 (the highest bit) of pixel blue color (RGB888) bit 5 (the highest bit) of pixel blue color (RX : RGB666) bit 3 of 12-bit transfer pixel color (RX)

Audio I/F

Pin	No	Type	Description
AC97_SYNC/ I2S0_WS/ EDM_TMS	M14	I/O	AC-Link sync output I2S0 word select I/O EDM TMS input
AC97_BITCLK/ I2S0_SCK/ EDM_TCK	L14	I/O	AC-Link bit clock input I2S0 sample clock I/O EDM TCK input
AC97_SDOUT/ I2S0_SD0/ EDM_TDI	N13	I/O	AC-Link data output I2S0 sample data lane-0 I/O EDM TDI input
AC97_SDIN/ I2S0_SD1/ EDM_TRST	M13	I/O	AC-Link data input I2S0 sample data lane-1 I/O EDM TRST input
N_AC97_RST/ I2S0_SD2/ EDM_TDO	L15	I/O	AC-Link reset output I2S0 sample data lane-2 I/O EDM TDO output
I2S0_SD3/ EXTGOICE	N11	I/O	I2S0 sample data lane-3 I/O EDM EXTGOICE input
I2S_MCLK/ EDM_DBGACK	N12	I/O	I2S0/I2S1 audio reference clock input EDM DBGACK output

SDRAM I/F

Pin	No	Type	Description
SCKE	G3	O	SDRAM clock enable
N_SRAS	A5	O	row address strobe
N_SCAS	C6	O	column address strobe
N_SWE	C7	O	write enable
SBS_0	B5	O	bit 0 of bank select address
SBS_1	C5	O	bit 1 of bank select address
SDQM0	A14	O	bit 0 of data mask
SDQM1	B6	O	bit 1 of data mask
SDQM2	E3	O	bit 2 of data mask
SDQM3	M3	O	bit 3 of data mask
SCLK	H1	O	SDRAM clock
SD_0	B14	I/O	bit 0 of data bus
SD_1	A13	I/O	Bit 1 of data bus
SD_2	B13	I/O	Bit 2 of data bus
SD_3	A12	I/O	Bit 3 of data bus
SD_4	B12	I/O	Bit 4 of data bus
SD_5	A11	I/O	Bit 5 of data bus
SD_6	B11	I/O	Bit 6 of data bus
SD_7	A10	I/O	Bit 7 of data bus
SD_8	B10	I/O	Bit 8 of data bus
SD_9	A9	I/O	Bit 9 of data bus
SD_10	B9	I/O	Bit 10 of data bus
SD_11	A8	I/O	Bit 11 of data bus
SD_12	B8	I/O	Bit 12 of data bus
SD_13	A7	I/O	Bit 13 of data bus
SD_14	B7	I/O	Bit 14 of data bus
SD_15	A6	I/O	Bit 15 of data bus
SD_16	D1	I/O	Bit 16 of data bus
SD_17	E1	I/O	Bit 17 of data bus
SD_18	E2	I/O	Bit 18 of data bus
SD_19	F1	I/O	Bit 19 of data bus
SD_20	G2	I/O	Bit 20 of data bus
SD_21	G1	I/O	Bit 21 of data bus
SD_22	F2	I/O	Bit 22 of data bus
SD_23	H2	I/O	Bit 23 of data bus
SD_24	J1	I/O	Bit 24 of data bus

SD_25	J2	I/O	Bit 25 of data bus
SD_26	K1	I/O	Bit 26 of data bus
SD_27	K2	I/O	Bit 27 of data bus
SD_28	L1	I/O	Bit 28 of data bus
SD_29	L2	I/O	Bit 29 of data bus
SD_30	M1	I/O	Bit 30 of data bus
SD_31	M2	I/O	Bit 31 of data bus
SA_0	A3	O	bit 0 of address bus
SA_1	B3	O	bit 1 of address bus
SA_2	C3	O	bit 2 of address bus
SA_3	A2	O	bit 3 of address bus
SA_4	B2	O	bit 4 of address bus
SA_5	C2	O	bit 5 of address bus
SA_6	A1	O	bit 6 of address bus
SA_7	B1	O	bit 7 of address bus
SA_8	C1	O	bit 8 of address bus
SA_9	D2	O	bit 9 of address bus
SA_10	A4	O	bit 10 of address bus
SA_11	B4	O	bit 11 of address bus
SA_12	C4	O	bit 12 of address bus

SDIO Host I/F

Pin	No	Type	Description
SD0_CMD	P6	IPUC/O	SDIO0 command
SD0_CLK	T7	O	SDIO0 clock output
SD0_D0	R7	IPUC/O	SDIO0 bit 0 of data bus
SD0_D1	P7	IPUC/O	SDIO0 bit 1 of data bus
SD0_D2	T8	IPUC/O	SDIO0 bit 2 of data bus
SD0_D3	R8	IPUC/O	SDIO0 bit 3 of data bus

SDIO Device I/F

Pin	No	Type	Description
SD1_CMD	R5	IPUC/O	SDIO1 command
SD1_CLK	T5	I	SDIO1 clock input
SD1_D0	P5	IPUC/O	SDIO1 bit 0 of data bus
SD1_D1	N5	IPUC/O	SDIO1 bit 1 of data bus
SD1_D2	T6	IPUC/O	SDIO1 bit 2 of data bus

SD1_D3	R6	IPUC/O	SDIO1 bit 3 of data bus

Blue Tooth UART (High Speed UART)

Pin	No	Type	Description
SOUT2/ GP10	N4	IPUC/O	Blue tooth UART serial output Bit 10 of GPIO port
NRTS2/ GP11	P4	IPUC/O	Blue tooth UART request to send output When low, this signal informs the modem or data set that the UART is ready to exchange data Bit 11 of GPIO port
SIN2/ GP12	R4	IPUC/O	Blue tooth UART serial input Bit 12 of GPIO port
NCTS2/ GP13	T4	IPUC/O	Blue tooth UART clear to send input When low, this signal indicates that a modem or data set is ready to exchange data. Bit 13 of GPIO port

Standard UART

Pin	No	Type	Description
SOUT4/ GP14	P3		

PWM

Pin	No	Type	Description
PWM0/ GP4	N9	IPUC/O	Panel backlight 0 Bit 4 of GPIO port
PWM1/ GP5	P9	IPUC/O	Panel backlight 1 Bit 5 of GPIO port

IR

Pin	No	Type	Description
IR0/ GP2	D11	IPU/O	IR0 data Bit 2 of GPIO port

I2C/DDC

Pin	No	Type	Description
I2C_SCLK/ SPI_CLK/ GP7	L13	IPUC/O	I2C sample clock in I2C mode. SPI clock in SPI mode while SPI1_SEL=0 and BOOT_TYPE=1. Bit 7 of GPIO port
I2C_SDA/ SPI_DI/ GP8	K13	IPUC/O	I2C data in I2C mode. SPI data input in SPI mode while SPI1_SEL=0 and BOOT_TYPE=1. Bit 8 of GPIO port group 0
DDC_SCLK/ GP20	K14	IPUC/O	DDC sample clock Bit 20 of GPIO port
DDC_SDA/ GP6	K15	IPUC/O	DDC data Bit 6 of GPIO port

MISCELLANENOUS

Pin	No	Type	Description
SPI1_SEL	D10	I	Pins selection for SPI interface (Please refer to the SPI pins selection)
ICE1_SEL	C11	I	Pins selection for ICE(EDM) interface (Please refer to the ICE (EDM) pins selection.)
SPI_CS/ ICE_I2S_SEL	C9	I/O	SPI chip select output ICE_I2S_SEL: Strap-pin during power on reset.

			1: Enable ICE interface while ICE1_SEL=0, 0: Enable AC97/I2S interface while ICE1_SEL=0.
CHIP_TYPE	C8	I	1: decoder mode, 0: encoder mode
BOOT_TYPE/ SPI_DO/ GP1	D9	IPUC/O	BOOT_TYPE: Strap-pin during power on reset. 1: Boot from SPI, 0: Boot from I2C SPI_DO: SPI data output Bit 1 of GPIO port
GP31	D8	I	SCAN_ENABLE for testing

SPI Pins Selection

Setting / SPI Signals	SPI1_SEL=1 BOOT_TYPE=1	SPI1_SEL=0 BOOT_TYPE=1
SPI_CLK	GP0	I2C_SCLK
SPI_DI	GP1	I2C_SDA
SPI_DO	BOOT_TYPE	BOOT_TYPE
SPI_CS	SPI_CS	SPI_CS

EDM (ICE) Pins Selection

Setting / EDM Signals	ICE1_SEL=0	ICE1_SEL=1
EDM_TCK	[redacted]	

6. Electric Characteristics

6. 1. Absolute Maximum Ratings

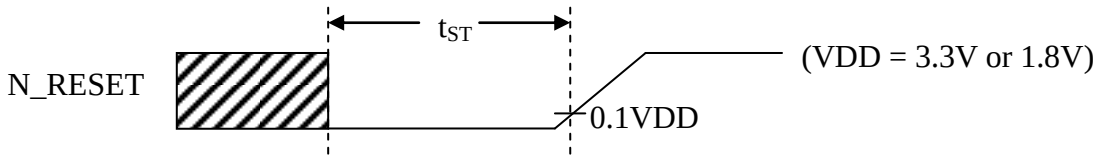
(VDD=3.3V or 1.8V, GND=0V)

Item	Symbol	Conditions	Rating	Unit
Ambient Temperature	TAB		0	

Low level output current@ V_{OL} = 0.45V		8mA	4.0	7.4	10.5	mA
		12mA	6.0	11.1	15.8	mA
Low level output current @V_{oL} =0.4V		8mA	8.4	13.3	16.3	mA
		12mA	12.6	19.9	24.4	mA
High level output current @V_{OH} = 1.35V		8mA	3.7	6.0	8.4	mA
		12mA	5.5	9.0	12.5	mA
High level output current @V_{oH} =2.4V		8mA	9.4	19.2	29.9	mA
		12mA	14.2	28.9	44.8	mA

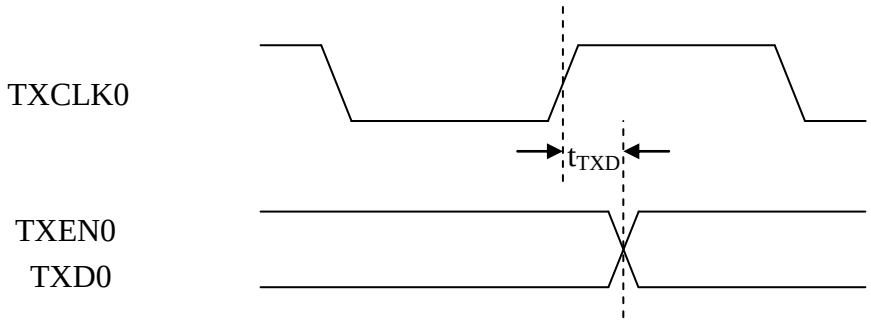
7. AC Characteristics Timing Chat

7. 1. Reset

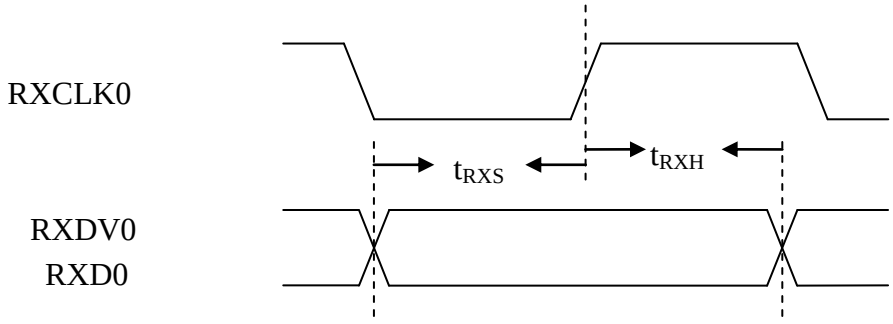


Item	Symbol	Min.	Max.	Unit
RESET time	t_{ST}	1	-	us

7. 2. MII Interface



Item	Symbol	Min.	Max.	Unit
MII output data delay time	t_{TXD}	-	20	ns



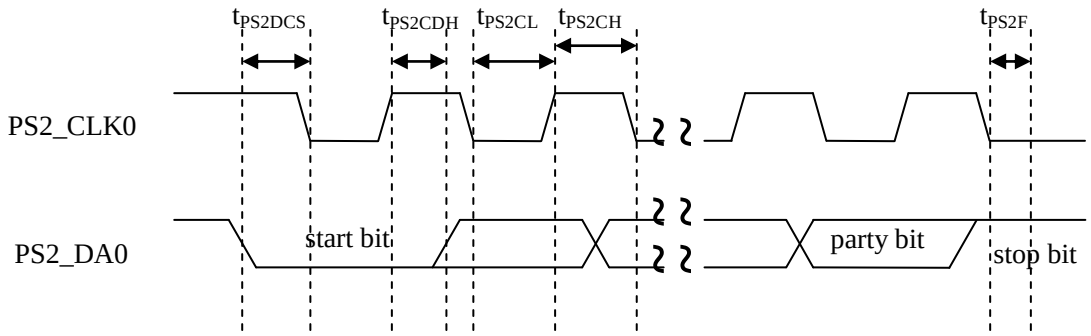
Item	Symbol	Min.	Max.	Unit
MII input data setup time	t_{RXS}	5	-	ns
MII input data hold time	t_{RXH}	2	-	ns

7. 3. MDC/MDIO Interface

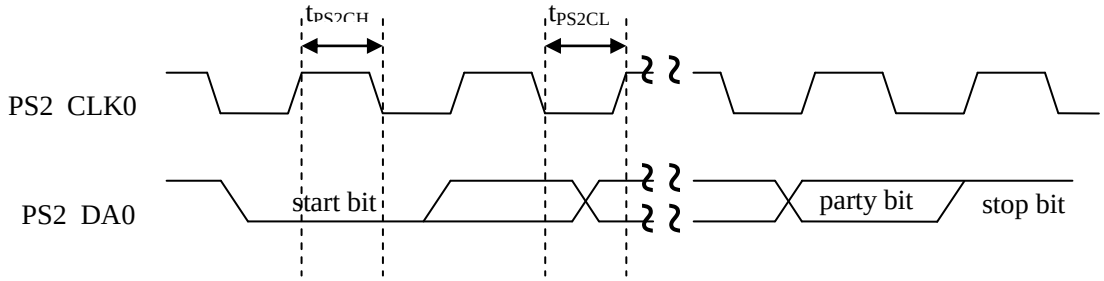
Item	Symbol	Min.	Max.	Unit
MDC/MDIO output data delay time	t_{MDO}	$(t_{cycle}/2)$	$(t_{cycle}/2)+5$	ns

Note: t_{cycle} is the cycle time of the MDC clock

7. 5. PS2 Interface

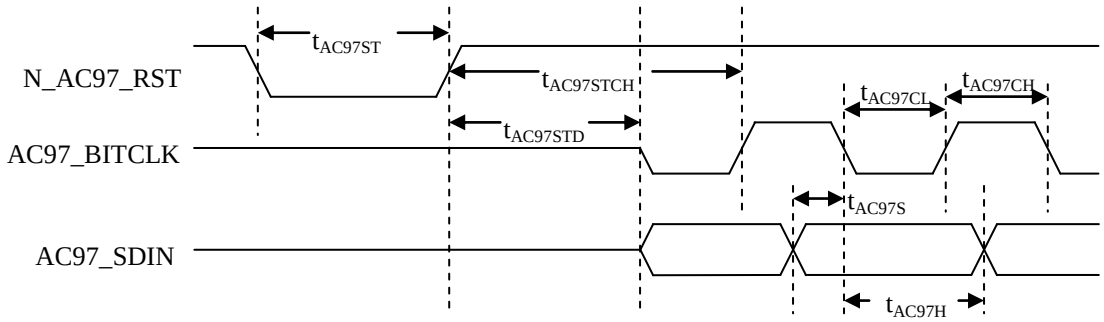


Item	Symbol	Min.	Max.	Unit
PS2 data to falling edge of clock setup time	t_{PS2DCS}	5	25	us
PS2 rising edge of clock to data hold time	t_{PS2CDH}	5	t_{PS2CH}-5	us
low period of the PS2 clock	t_{PS2CL}	30	50	us
high period of the PS2 clock	t_{PS2CH}	30	50	us
PS2 does not start another transmission time	t_{PS2F}	~0	50	us
PS2 byte receive time		-	1.1	ms

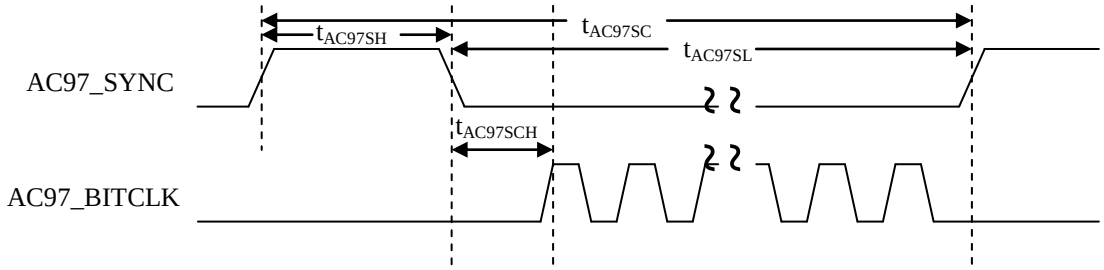


Item	Symbol	Min.	Max.	Unit
low period of the PS2 clock	t_{PS2CL}	30	50	us
high period of the PS2 clock	t_{PS2CH}	30	50	us
PS2 byte send time		-	1.1	ms

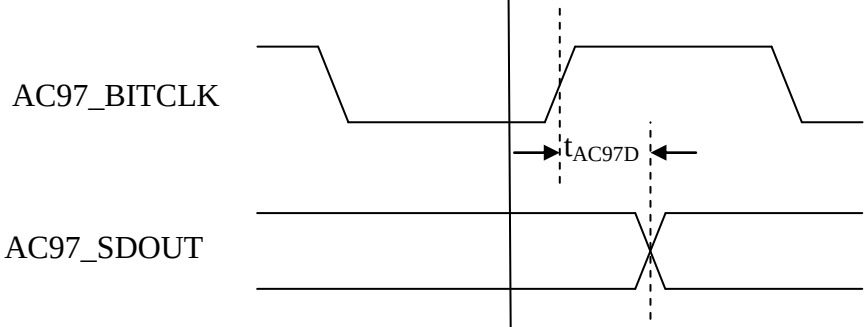
7. 6. AC97 Interface



Item	Symbol	Min.	Max.	Unit
AC97 reset time	t_{AC97ST}	1	-	us
AC97 reset de-assert to bitclk or sdin active	$t_{AC97STD}$	-	25	ns
AC97 reset de-assert to bitclk rising	$t_{AC97STCH}$	163	400	ns
low period of the AC97 bitclk	t_{AC97CL}	36	45	ns
high period of the AC97 bitclk	t_{AC97CH}	36	45	ns
AC97 input data setup time	t_{AC97S}	10	-	ns
AC97 input data hold time	t_{AC97H}	10	-	ns

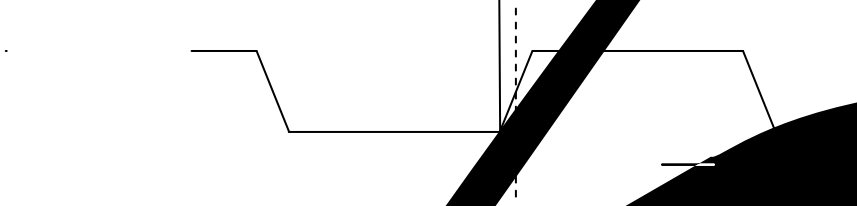


Item	Symbol	Min.	Max.	Unit
Period of the AC97 sync	t_{AC97SC}	20	-	us
High period of the AC97 sync	t_{AC97SH}	1	-	us
Low period of the AC97 sync	t_{AC97SL}	19	-	us
AC97 sync de-assert to bitclk rising	$t_{AC97SCH}$	163	-	ns



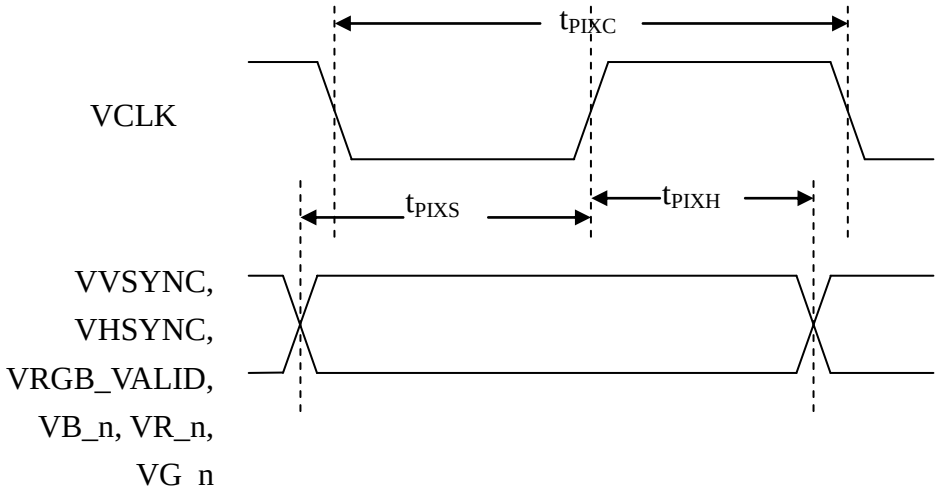
Item	Symbol	Min.	Max.	Unit
AC97 output data delay time	t_{AC97D}		15	ns

7. 7. I2S Interface



				ns
			-	ns
		10	-	ns
		60	-	ns
	t_{IISH}	0	-	ns

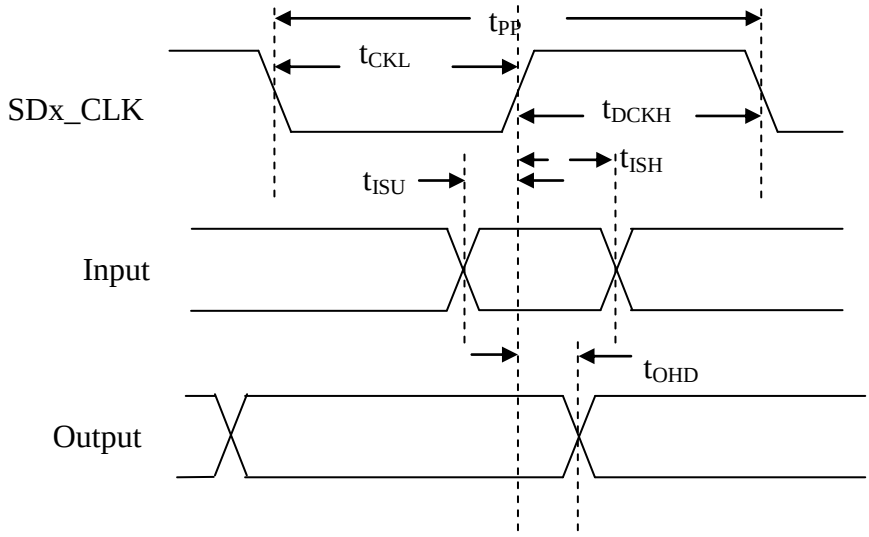
7. 8. Video Interface



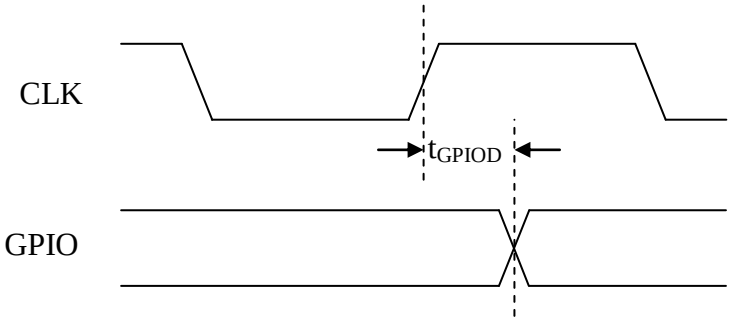
Item	Symbol	Min.	Max.	Unit
Period of the video pixel clock	t_{PIXC}	6	-	ns
Video input data and control setup time	t_{PIXS}	2	-	ns
Video input data and control hold time	t_{PIXH}	1	-	ns

7. 9. SDIO Interface

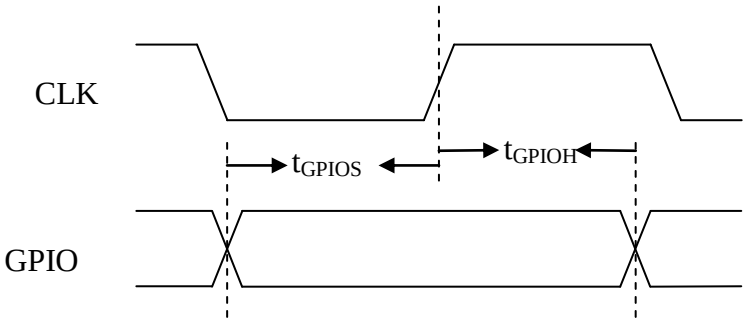
25MHz timing chart



7. 10. GPIO Interface

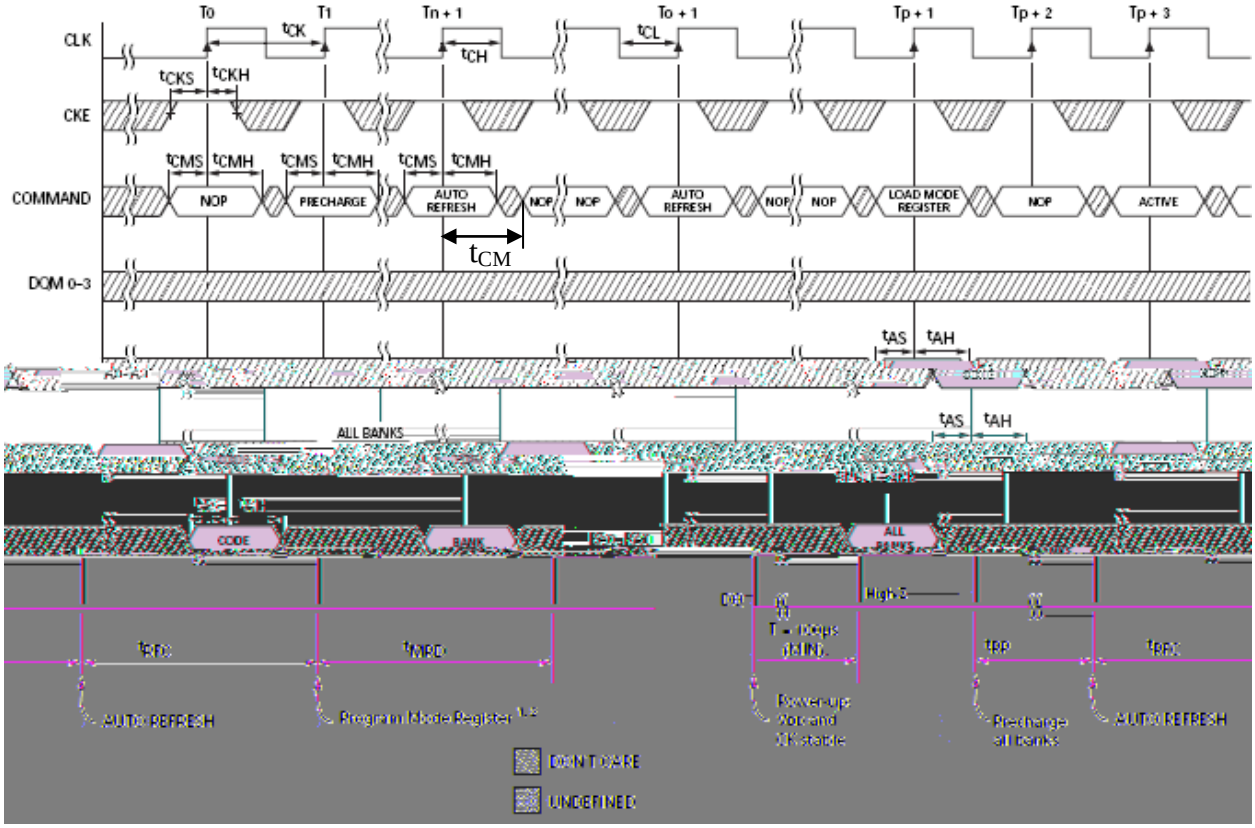


Item	Symbol	Min.	Max.	Unit
GPIO output high data delay time	t_{GPIOD}	9	-	ns
GPIO output low data delay time	t_{GPIOD}	3	-	ns

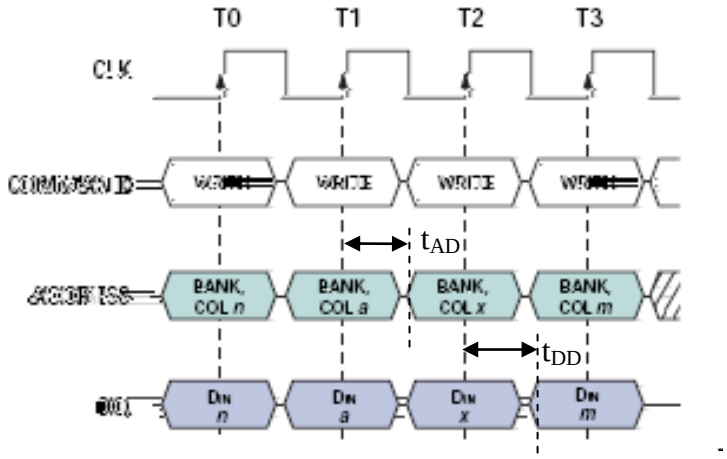


Item	Symbol	Min.	Max.	Unit
GPIO input data setup time	t_{GPIOS}	5	12	ns
GPIO input data hold time	t_{GPIO}	5	12	ns

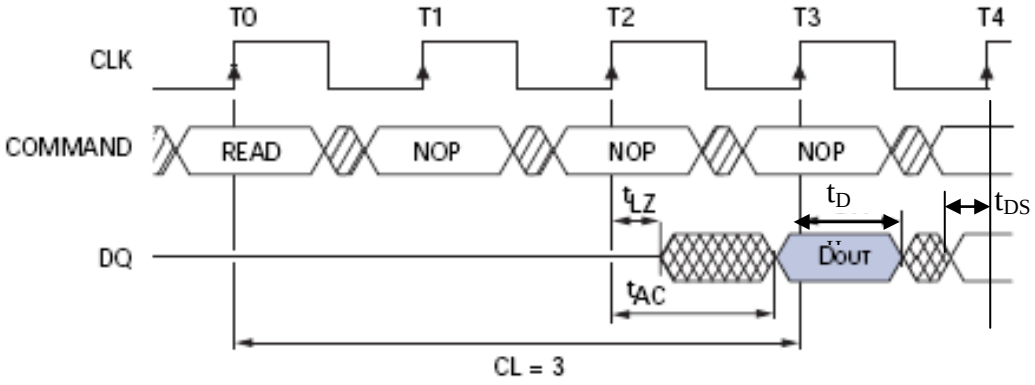
7. 11. SDRAM Interface



Item	Symbol	Min.	Max.	Unit
Period of the SDAM clock	t_{CK}	6	-	ns
High period of the SDAM clock	t_{CH}	2.8	-	ns
Low period of the SDAM clock	t_{CL}	3	-	ns
SDRAM output RAS, CAS, WE delay time	t_{CMD}	2.65	4.35	ns
Auto refresh time	t_{RFC}	26	52	us



Item	Symbol	Min.	Max.	Unit
SDRAM output RAS, CAS, WE delay time	t_{CMD}	2.65	4.35	ns
SDRAM output address delay time	t_{AD}	2.45	4.3	ns
SDRAM output data delay time	t_{DD}	1	4.5	ns



Item	Symbol	Min.	Max.	Unit
SDRAM input data setup time	t_{DS}	0.5	-	ns
SDRAM input data hold time	t_{DH}	0	-	ns

8. Guidelines

8.1 Layout Guide

There are some generic constrains for PCB layout and manufacturing. For other device specific constrains, please refer datasheets provided by venders or the documentation: TF-680 PCB Layout guide.doc .

I. Recommend 4-layer PCB stack up
   - ✓ Layer 1 for signal
   - ✓ Layer 2 for ground
   - ✓ Layer 3 for power
   - ✓ Layer 4 for signal

II. Clock signal
   - ✓ All of the Clock signals must be routing on the TOP layer of PCB, no via and shorten the clock trace as possible

III. Power supply decoupling
   - ✓ Decoupling capacitors should be connected as close as possible to their respective power and ground
   - ✓ Short and wide trace
   - ✓ Ground pins should connect directly to its respective decoupling capacitor ground lead; then connected to the ground plane through a ground via
   - ✓ DO NOT connect the power pins of BGA chip to power plane through vias directly. The power traces should be connected to power plane on one side, and connect the other side to bypass capacitors before connect them to power pins of chip

IV. SDRAM interface
   - ✓ The Clock signal of SDRAM (MCLK/MCKE) signal should be routing on the Top layer, and Spacing between data bus trace and clock trace> 20 mil
   - ✓ The trace clearance must > the stackup thickness of L1 and L2
   - ✓ Spacing the clock trace and the PLL power >20 mil

V. Crystal constraints
   - ✓ Must be placed as close as possible to the XI, XO pins
   - ✓ Overlaying the ground plane
   - ✓ The ground reference of the external capacitors connected to the crystal pins must be connected very close to the ground
   - ✓ High speed traces should not be routed under or adjacent these pins

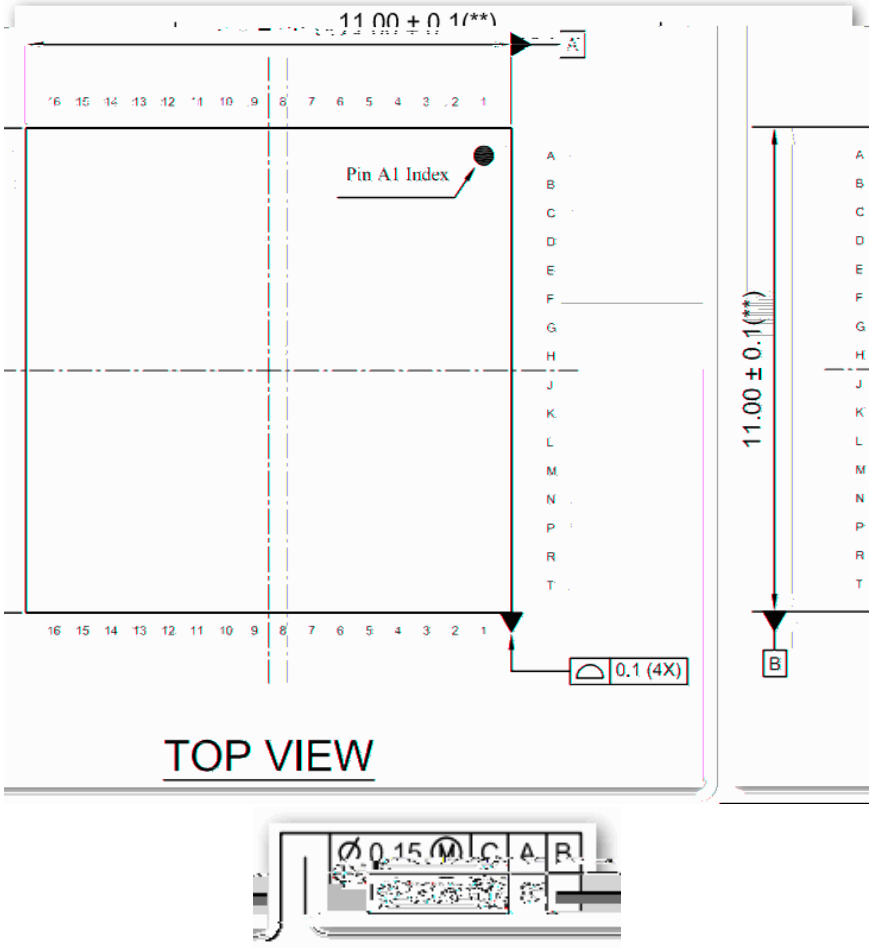
8.2 Power on Sequence

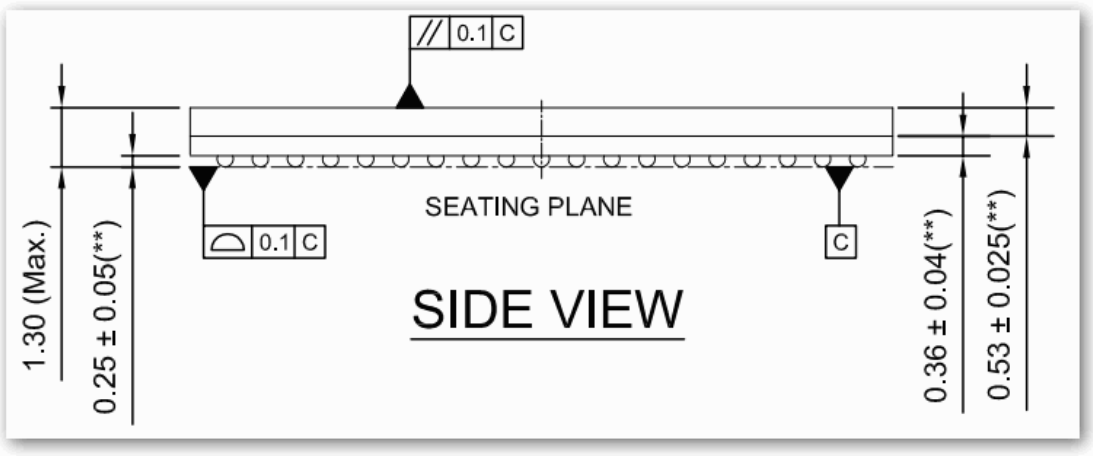
The guide line is the PAD power should be ready before the Core power. For TF680, there are 3.3V for PLL PAD powers, 3.3/1.8V for other PAD power. These powers should lead before the Core power 1.2V. If you do not follow the sequence, the PAD may enter latch-up state. The chip will not enter normal state.

The proposal for the delay of PAD power to Core power is less than 1ms. The long delay time may reduce the chip life.

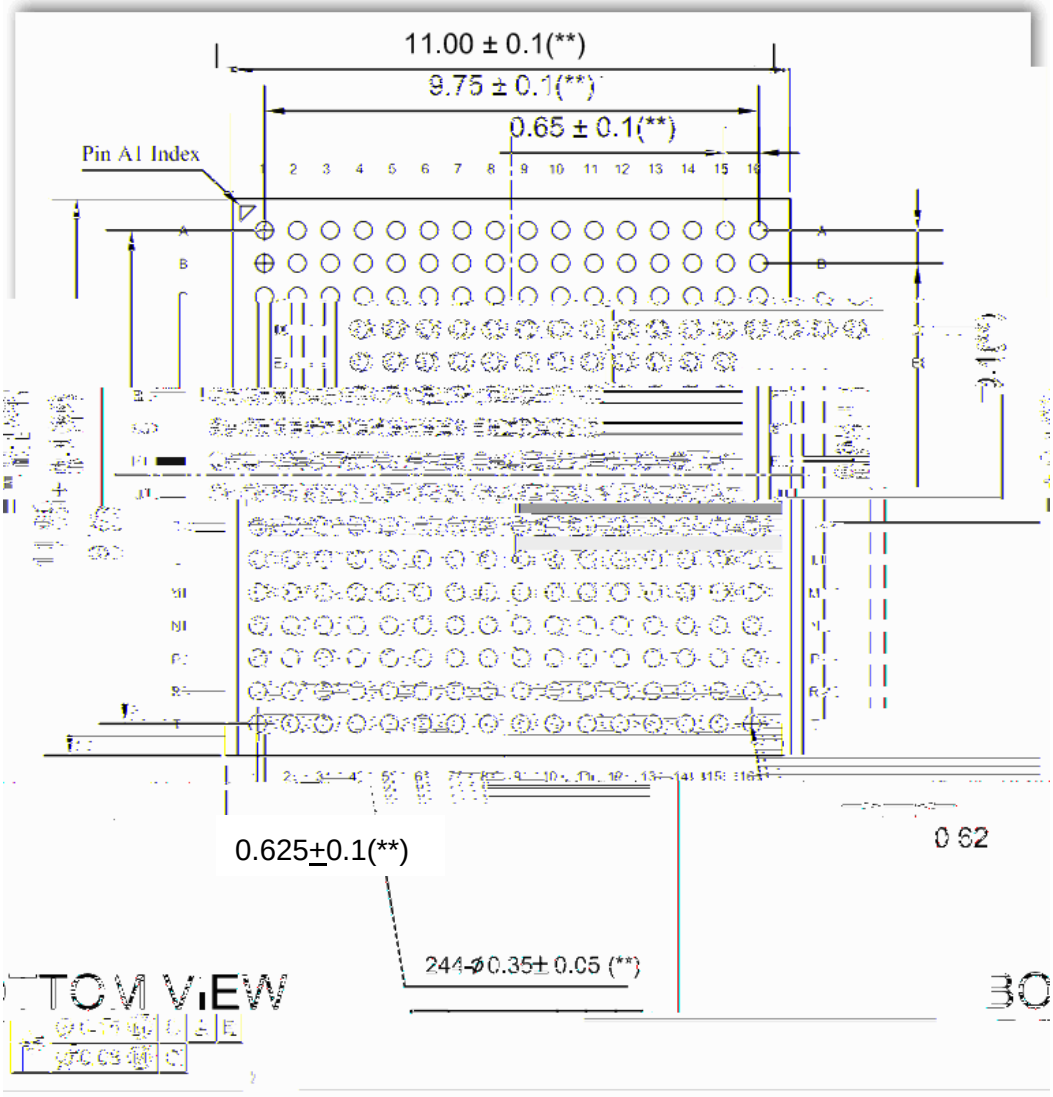
9. Mechanical Drawing

Unit in mm

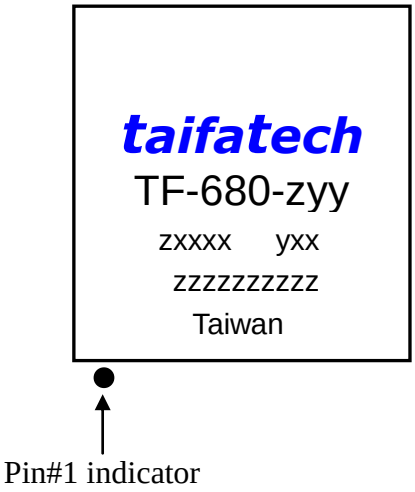



0.1 C
SEATING PLANE
0.1 C
C
SIDE VIEW
1.30 (Max.)
0.25 ± 0.05(**)
0.36 ± 0.04(**)
0.53 ± 0.025(**)

Ø 0.15 M C A B


11.00 ± 0.1(**)
9.75 ± 0.1(**)
0.65 ± 0.1(**)
Pin A1 Index
0.625±0.1(**)
0.62
244-Ø0.35± 0.05 (**)

10. Marking Rule

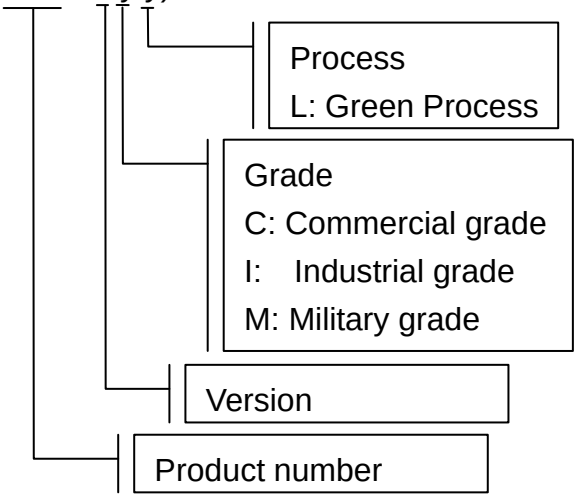


x represents a number from 1 to 9 and y represents an alphabet from A to Z.

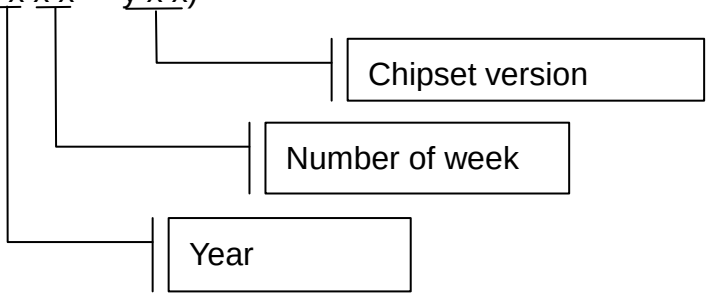
Marking information

Line 1: Company name ***(taifatech)***

Line 2: Product number (T F - 6 8 0 - z y y)



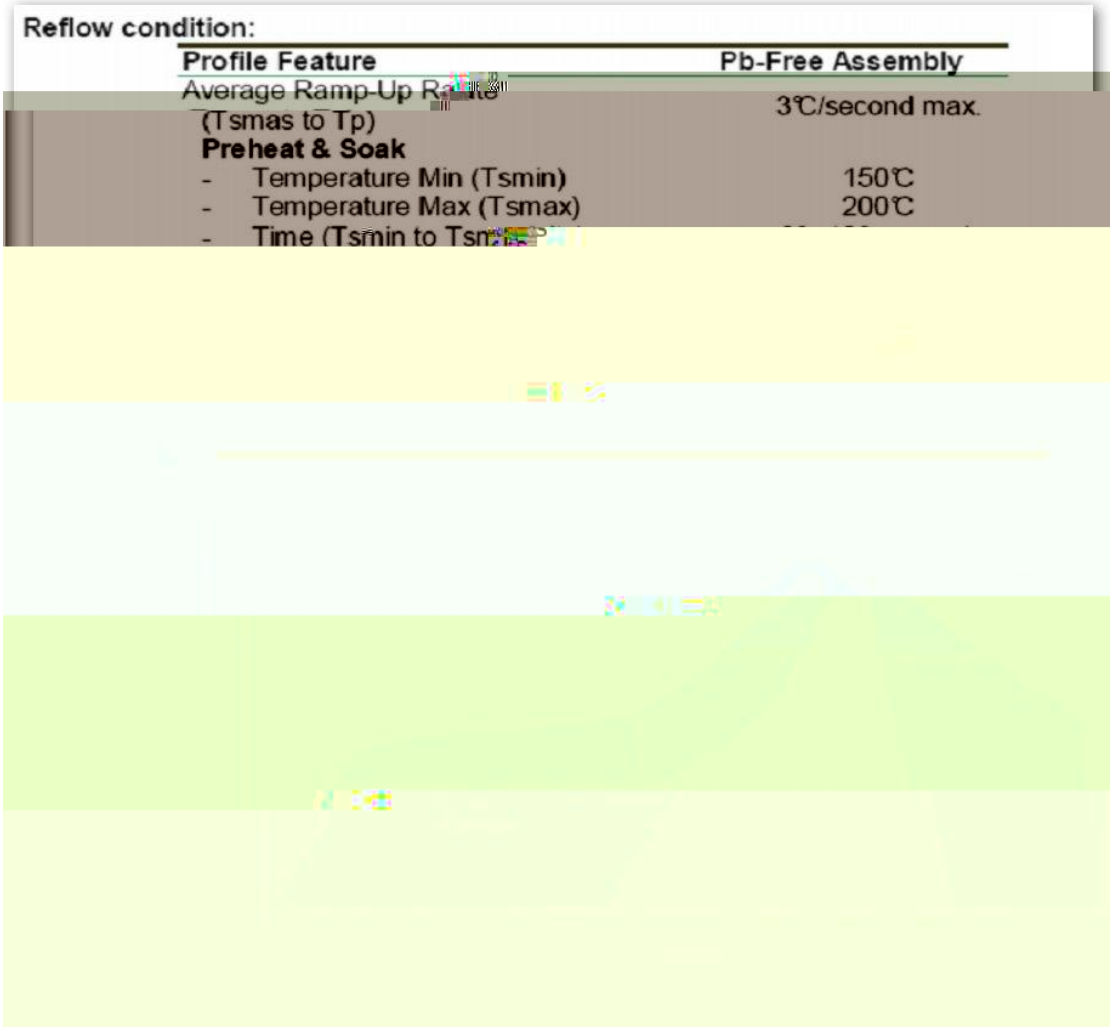
Line 3: Date code (z x x x x y x x)



Line 5: Country (Taiwan)

11. Application Note

11.1 Reflow Condition



Reflow condition:

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmas to Tp)	3℃/second max.
Preheat & Soak	
- Temperature Min (Tsmin)	150℃
- Temperature Max (Tsmax)	200℃
- Time (Tsmin to Tsmax)	

11.2 SMT Assembly Recommendations

This document is intended to help to yield high quality for the solder attachment of TFBGA ball pins. If customers cannot meet/follow all of the recommendations, they should contact Taifatech to discuss the best alternatives.

I. IR reflow condition

- Please refer to J-STD-020D1 as defined in *11.1 Reflow Condition* .

II. Solder paste

- Please choose the solder paste with melting point near 217 (the melting point of solder ball, composition: SAC405).

III. Location tolerance of SMT

- The location tolerance for ball size 0.35mm TFBGA is +/- 0.11mm. SMT

location misalignment for TF680 should be no more than 0.11mm.